

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

16. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW;

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error; and

a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator and [The phase-locked system according to claim 15] wherein the transfer path gain is dependent upon a reference frequency  $f_{ref}$  and an estimated digitally-controlled oscillator gain  $\hat{K}_{DCO}$ , is

functionally defined as  $\frac{f_{ref}}{\hat{K}_{DCO}}$ .

### **REMARKS**

Claims 1-10, 17-23 and 25 stand allowed. Objected to Claim 16 has been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Claim 16 stands allowable.

Claims 11-15 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over